

What is claimed is:

1. A process of designing an integrated circuit comprising:
determining a specification for the integrated circuit;
mapping functions to the specification, the functions being
comprised of groups; and
determining the placement of the functions in a layout.
2. The process of designing an integrated circuit of claim 1 wherein
the functions are of a plurality of predefined sizes and shapes.
3. The process of designing an integrated circuit of claim 2 wherein
the groups are of a plurality of predefined sizes and shapes.
4. The process of designing an integrated circuit of claim 3 wherein
the groups have predefined interconnection points.
5. The process of designing an integrated circuit of claim 4 wherein
the groups each provide one of a plurality of logic functions.
6. The process of designing an integrated circuit of claim 5 wherein
multiple groups, each of a different size and shape, provide the same logic function.
7. The process of designing an integrated circuit of claim 6 further
comprising mapping groups to the specification and determining placement of the groups
in the layout.
8. The process of designing an integrated circuit of claim 7 wherein
the groups define a physical representation of a logic circuit.
9. The process of designing an integrated circuit of claim 8 wherein
the groups are defined by GDSIII files.
10. The process of designing an integrated circuit of claim 9 wherein
the groups are comprised of on the order of 1000 gates.
11. A method of determining a definition of a physical representation
of at least a portion of an integrated circuit, the integrated circuit performing logic

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Sub A-1

operations, arithmetic operations, control operations, and memory operations, the integrated circuit being comprised of a plurality of groups, the groups being largely comprised of between 300 and 5000 gates, the groups being present in a library of groups, with each group being predefined in terms of logical and physical layouts, the physical layouts having predefined boundaries with predefined interconnection points along the physical boundaries, and at least some of the groups being amalgamated into functions, the functions being present in a library of function, the method comprising:

selecting an item, the item being a group or a function, for placement on a layout;
 placing the item on the layout;
 selecting a further item for placement on the layout;
 placing the further item on the layout; and
 defining interconnections between the item and the further item.

12. The method of claim 11 wherein the layout comprises a plurality of layers.

13. The method of claim 12 wherein the plurality of layers are separated by metalization having vias.

14. An integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit groups having predefined connection points, at least some of the circuit groups being amalgamated into sets of groups.

15. The integrated circuit of claim 14 further comprising trailers attached to groups.

16. The integrated circuit of claim 15 wherein the trailers provide physical translation of interface signals associated with the predefined connection points.

17. The integrated circuit of claim 15 wherein the trailers provide for buffering of interface signals associated with the predefined connection points.

18. The integrated circuit of claim 15 wherein the trailers provide for staging of interface signals associated with the predefined connections points.

Sub A-1
Cont'd

Sub A-2
FIG. 10

27. A process of designing an electronic logic system, the process comprising:

mapping groups to a functional description, the groups being comprised of up to 5000 gates, the groups being partitioned into data path groups, control groups, memory groups, I/O groups, and analog groups;

testing functional models of the mapped groups to verify the functional correctness of the mapping of groups to the functional description;

8 performing timing, area, and power estimation using detailed
9 physical models of the mapped groups; and
10 importing implementation files into the design.

1 28. The process of designing an electronic logic system of claim 27
2 wherein the groups are predefined in terms of behavior, timing, power, and physical
3 layout.

1 29. The process of designing an electronic logic system of claim 28
2 wherein different sets of groups implement different functions.

1 30. The process of designing an electronic logic system of claim 29
2 wherein groups within a set of groups implementing a function implement different
3 behavior.

1 31. The process of designing an electronic logic system of claim 29
2 wherein groups within a set of groups implementing a function have different physical
3 layouts.

1 32. The process of designing an electronic logic system of claim 29
2 wherein groups within a set of groups implementing a function have different power
3 usage.

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